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appropriate voltage levels are not normally applied, and further wherein the spare cells within a particular block are substituted in place of any defective cells within said plurality of cells of said particular block.

1022. The method of any one of claims 1, 63-71, carried out on a single integrated circuit chip.--

REMARKS

The present application, at page 11, lines 27-31, incorporates by reference another application entitled "Multi-State EEprom Read and Write Circuits and Techniques", filed on the same day as the initial parent to the present application, namely April 13, 1989, by Sanjay Mehrotra and Eliyahou Harari, two of the inventors who are also named in the present application. This incorporated application is Serial No. 07/337,579, now abandoned, continuations-in-part of which have issued as patents nos. 5,163,021 and 5,172,338. A primary purpose of the present amendment is to insert a majority of the incorporated Serial No. 07/337,579 into the present application in order to support claims based thereon that are also being added by this Preliminary Amendment.

Therefore, essentially all of the Summary of the Invention, Brief Description of the Drawings and Description of the Preferred Embodiments sections of Serial No. 07/337,579 are being added to the present application. A major revision that has been made to this added text is a change in the drawing figure numbers. Figures 1-17 of Serial No. 07/337,579 are being renumbered herein as figures 9-25, respectively, in order not to use any of the same figure numbers previously used in the present application. Tables 1 and 2 of the incorporated application have also been relabeled as figures 26 and 27, respectively. Further, the reference numbers of the drawings have been changed by adding 1000 to the reference numbers of the figures being incorporated from Serial No. 07,337,579, in order to avoid duplicating the reference numbers already used in the original figures of the present application. Corresponding changes have been made to the text of Serial No. 07/337,579 that is being inserted into the present application.

The claims being substituted into this application are directed to inhibiting, cell by cell, further application of voltages to a plurality of cells when the individual cells are verified to have reached their desired states. System claims 27-34, 40-42 and 44 of U.S. patent no. 5,172,338 are directed to similar subject matter with a different scope. In response to the request of SanDisk Corporation, the common owner of the present application and the '338 patent, for reexamination of claims 27 and 32 of patent no. 5,172,338, Reexamination No. 90/004,352 has been instituted. Also, pursuant to the request of third party Samsung Corporation, patent no. 5,172,338 is the subject of Reexamination No. 90/004,387. Both reexaminations are being conducted in Group Art Unit 2511.

Patent no. 5,172,338 is currently involved in the following litigation between SanDisk and Samsung:

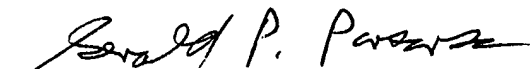
Samsung Electronics Co., Ltd. v. SanDisk Corporation,
United States District Court for the Northern District of California, Case No. C95-03512DLT; and

In the Matter of Certain Flash Memory Circuits and Products Containing Same, United States International Trade Commission (ITC), Investigation No. 337-TA-382.

A prompt examination and allowance of the present continuation application is solicited.

Dated: December 20, 1996

Respectfully submitted,



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